

without departing from the spirit and scope of the invention.

What is claimed is:

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1. A method to pattern a polysilicon layer in the manufacture of an integrated circuit device comprising:

providing a polysilicon layer overlying a semiconductor substrate;

5 providing a hard mask layer overlying said polysilicon layer;

providing a resist layer overlying said hard mask layer;

patterning said resist layer to form a resist mask that exposes a part of said hard mask layer;

10 patterning said polysilicon layer wherein said patterning is performed sequentially in a dry plasma etch chamber and wherein said patterning comprises:

etching said hard mask layer exposed by said resist mask to form a hard mask that exposes a part of said polysilicon layer;

15 thereafter stripping away said resist mask;

thereafter cleaning away polymer residue from said ~~resist~~ ^{hard} mask wherein said cleaning away comprises a chemistry containing CF_4 gas; and

20 thereafter etching said polysilicon layer exposed by said hard mask; and

stripping away said hard mask to complete the patterning of said polysilicon layer in the manufacture of the integrated circuit device.

2. The method according to Claim 1 wherein said hard mask layer comprises silicon oxynitride.

3. The method according to Claim 1 wherein said step of etching said hard mask layer comprises a chemistry containing CF_4 gas.

4. The method according to Claim 1 wherein said step of stripping away said resist mask comprises a chemistry containing O_2 gas.

5. The method according to Claim 1 wherein said step of etching said polysilicon layer comprises a main etch step followed by an overetch step.

6. The method according to Claim 1 wherein said step of etching said polysilicon layer comprises a chemistry of: HBr gas, Cl_2 gas, He-O_2 gas, and combinations thereof.

7. The method according to Claim 1 further comprising providing a silicon dioxide layer overlying said hard mask layer and underlying said resist layer.

8. The method according to Claim 1 further comprising etching

said resist layer to trim said resist layer prior to said step of etching said hard mask layer wherein said etching of said resist layer is performed in said dry plasma etching chamber.

9. A method to pattern a polysilicon layer in the manufacture of an integrated circuit device comprising:

providing a polysilicon layer overlying a semiconductor substrate;

5 providing a hard mask layer overlying said polysilicon layer;

providing a resist layer overlying said hard mask layer;
patterning said resist layer to form a resist mask that exposes a part of said hard mask layer;

10 patterning said polysilicon layer wherein said patterning is performed sequentially in a dry plasma etch chamber and wherein said patterning comprises:

etching said resist mask to trim said resist mask;

thereafter etching said hard mask layer exposed by
15 said resist mask to form a hard mask that exposes a part of said polysilicon layer;

thereafter stripping away said resist mask;

thereafter cleaning away polymer residue from said resist mask wherein said cleaning away comprises a
20 chemistry containing CF_4 gas; and

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thereafter etching said polysilicon layer exposed by
said hard mask; and
stripping away said hard mask to complete the patterning
of said polysilicon layer in the manufacture of the integrated
circuit device.

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10. The method according to Claim 9 wherein said hard mask
layer comprises silicon oxynitride.

11. The method according to Claim 9 wherein said step of
etching said resist mask to trim said resist mask comprises a
chemistry containing O_2 gas.

12. The method according to Claim 9 wherein said step of
etching said hard mask layer comprises a chemistry of CF_4 gas.

13. The method according to Claim 9 wherein said step of
stripping away said resist layer comprises a chemistry
containing O_2 gas.

14. The method according to Claim 9 wherein said step of
etching said polysilicon layer comprises a main etch step
followed by an overetch step.

15. The method according to Claim 9 wherein said step of

etching said polysilicon layer comprises a chemistry of: HBr gas, Cl₂ gas, He-O₂ gas, and combinations thereof.

16. The method according to Claim 1 further comprising providing a silicon dioxide layer overlying said hard mask layer and underlying said resist layer.

17. A method to pattern a polysilicon layer in the manufacture of an integrated circuit device comprising:

providing a gate oxide layer overlying a semiconductor substrate;

providing a polysilicon layer overlying said gate oxide layer;

providing a silicon oxynitride layer overlying said polysilicon layer;

providing a silicon dioxide layer overlying said silicon dioxide layer;

providing a resist layer overlying said silicon dioxide layer;

patterning said resist layer to form a resist mask that exposes a part of said silicon oxynitride layer;

patterning said polysilicon layer wherein said patterning is performed sequentially in a dry plasma etch chamber and wherein said patterning comprises:

etching said resist mask to trim said resist mask;

20 thereafter etching said silicon dioxide layer and
said silicon oxynitride layer exposed by said resist mask
to form a hard mask that exposes a part of said
polysilicon layer;

thereafter stripping away said resist mask;

25 thereafter cleaning away polymer residue from said
resist mask wherein said cleaning away comprises a
chemistry containing CF_4 gas; and

thereafter etching said polysilicon layer exposed by
said hard mask wherein said etching comprises a main etch
step followed by an overetch step; and

30 stripping away said hard mask to complete the patterning
of said polysilicon layer in the manufacture of the integrated
circuit device.

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18. The method according to Claim 17 wherein said step of
etching said silicon dioxide layer and said silicon oxynitride
layer comprises a chemistry of CF_4 gas.

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19. The method according to Claim 17 wherein said step of
stripping away said resist layer comprises a chemistry
containing O_2 gas.

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20. The method according to Claim 17 wherein said step of

